

DRAFT

**A Four Channel Optical Receiver Mezzanine Module
and
A Four Channel Optical Transmitter Mezzanine Module**

**Which is to be used on the
Stereo Finder System**

**and
be Compatible with the CDF Pulsar Module**

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INTRODUCTION

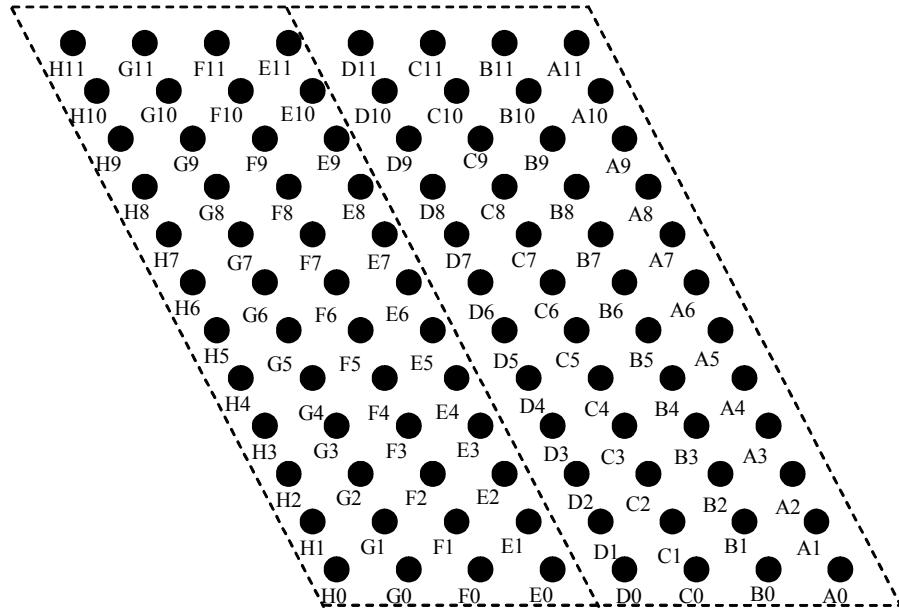
Stereo XFT Data Source

The sources of the XFT data are TDC modules. Each of these modules contain timing information for 96 wires. The TDC produces 6 bits of data for each wire. This data identifies whether a wire has a “hit” on it for a particular time slice. There are 6 identified time slices within each 396ns period, or 3 CDF_Clock cycles.

In addition to sending up the hit information for each wire, it is desirable to tag the information with a Beam_Zero marker, to identify its position in time as well as some type of identification tag to mark the source of the data.

The plan is to send the data from the TDC modules to the XFT modules via an 8B/10B encoded serial optical bitstream. Furthermore, we would like to limit the data rate on such a link to ~1.25Gbps which is supported by a wide variety of commercial products available for Gigabit Ethernet.

The following tables show the data packing using a 16 bit SERDES part, the TI TLK1501. Each TDC Transition module would need to drive 2 optical fibers, each carrying the data from 48 wires. In some cases, the TDC transition module must drive a copy of one data set to allow for neighbor sharing on different XFT Stereo modules.



Naming Convention of the 96 TDC Wires

Data Fiber # 1 carries information from TDC wires 0-47

Data Word	Beam_Zero Marker 1 bit	Word Zero Flag 1 bit	Group Identifies 2 bits	Wire data time slice (0-5) 12 bits
1	beam_zero	1	00	t0 (A0-A11)
2	beam_zero	1	01	t0 (B0-B11)
3	beam_zero	1	10	t0 (C0-C11)
4	beam_zero	1	11	t0 (D0-D11)
5	beam_zero	0	00	t1 (A0-A11)
6	beam_zero	0	01	t1 (B0-B11)
7	beam_zero	0	10	t1 (C0-C11)
8	beam_zero	0	11	t1 (D0-D11)
9	beam_zero	0	00	t2 (A0-A11)
10	beam_zero	0	01	t2 (B0-B11)
11	beam_zero	0	10	t2 (C0-C11)
12	beam_zero	0	11	t2 (D0-D11)
13	beam_zero	0	00	t3 (A0-A11)
14	beam_zero	0	01	t3 (B0-B11)
15	beam_zero	0	10	t3 (C0-C11)
16	beam_zero	0	11	t3 (D0-D11)
17	beam_zero	0	00	t4 (A0-A11)
18	beam_zero	0	01	t4 (B0-B11)
19	beam_zero	0	10	t4 (C0-C11)
20	beam_zero	0	11	t4 (D0-D11)
21	beam_zero	0	00	t5 (A0-A11)
22	beam_zero	0	01	t5 (B0-B11)
23	beam_zero	0	10	t5 (C0-C11)
24	beam_zero	0	11	t5 (D0-D11)

Data Fiber # 2 carries information from TDC wires 48-95

Data Word	Beam_Zero Marker 1 bit	Word Zero Flag 1 bit	Group Identifies 2 bits	Wire data time slice (0-5) 12 bits
1	beam_zero	1	00	t0 (E0-E11)
2	beam_zero	1	01	t0 (F0-F11)
3	beam_zero	1	10	t0 (G0-G11)
4	beam_zero	1	11	t0 (H0-H11)
5	beam_zero	0	00	t1 (E0-E11)
6	beam_zero	0	01	t1 (F0-F11)
7	beam_zero	0	10	t1 (G0-G11)
8	beam_zero	0	11	t1 (H0-H11)
9	beam_zero	0	00	t2 (E0-E11)
10	beam_zero	0	01	t2 (F0-F11)
11	beam_zero	0	10	t2 (G0-G11)
12	beam_zero	0	11	t2 (H0-H11)
13	beam_zero	0	00	t3 (E0-E11)
14	beam_zero	0	01	t3 (F0-F11)
15	beam_zero	0	10	t3 (G0-G11)
16	beam_zero	0	11	t3 (H0-H11)
17	beam_zero	0	00	t4 (E0-E11)
18	beam_zero	0	01	t4 (F0-F11)
19	beam_zero	0	10	t4 (G0-G11)
20	beam_zero	0	11	t4 (H0-H11)
21	beam_zero	0	00	t5 (E0-E11)
22	beam_zero	0	01	t5 (F0-F11)
23	beam_zero	0	10	t5 (G0-G11)
24	beam_zero	0	11	t5 (H0-H11)

Suggested link fiber specifications

Graded input multimode fiber (Ge doped), 50/125µm, 850nm

Manufactures of such fiber include Corning and Alcoa

LC ends at both ends

Require testing data showing attenuation with 850nm source

Suggested parts used to implement this data link

SERDES part: TI TLK1501 (0.6 TO 1.5 GBPS TRANCEIVER)

E/O part: Stratos Lightwave M2T-25-4-1-L (850nm SFF LC 2x5 Dual Transmitters)

O/E part: Stratos Lightwave M2R-25-4-1-TL (850nm SFF LC 2x5 Dual Receivers)

Clocking and Synchronization issues

“Idle” patterns should be sent up these links during abort gaps so that any links with synchronization problems will be able to automatically re-sync. An “Idle” pattern is easily created through the use of the transmit data control bits of the Serdes transmitter

The clocking of the Serdes part is done with a period of $396\text{ns} \div 24 = 16.5\text{ns}$. This is a frequency of 60.6060MHz. It is also CDF_Clock multiplied by 8.

It is important to keep in mind that the pk-pk jitter spec on the Serdes part is 40ps. This is tough to achieve with a PLL and care will need to be taken and studies done to determine if this will work for us. (An alternative would be to use an Oscillator which runs faster, 62.500Mhz. We would then need to re-synchronize back to the CDF_Clock timings.)

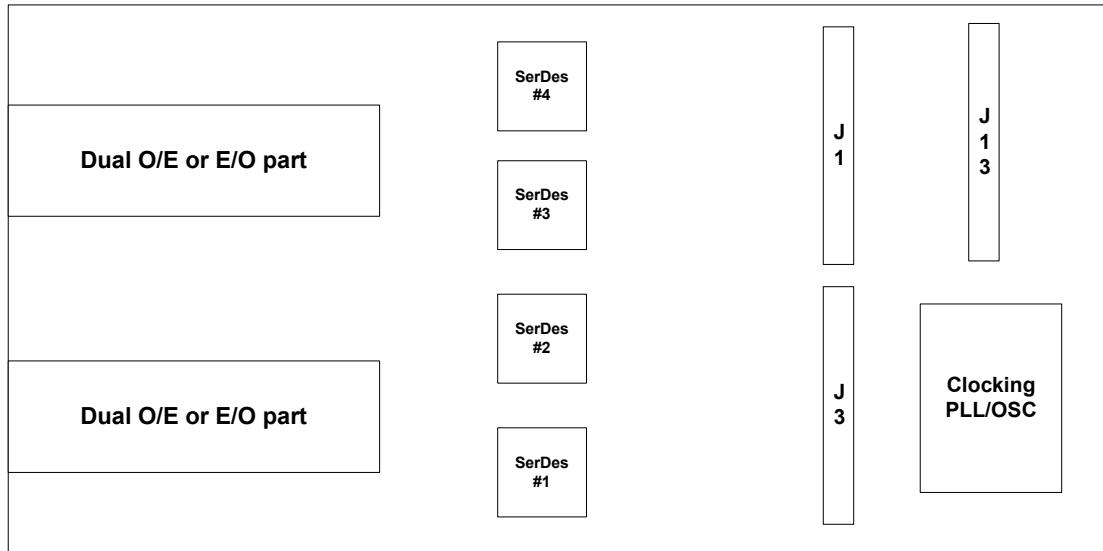
A possible PLL choice for our application is Integrated Circuit Systems ICS670-01.

A possible Oscillator choice is Raltron C04610-66.500-TR.

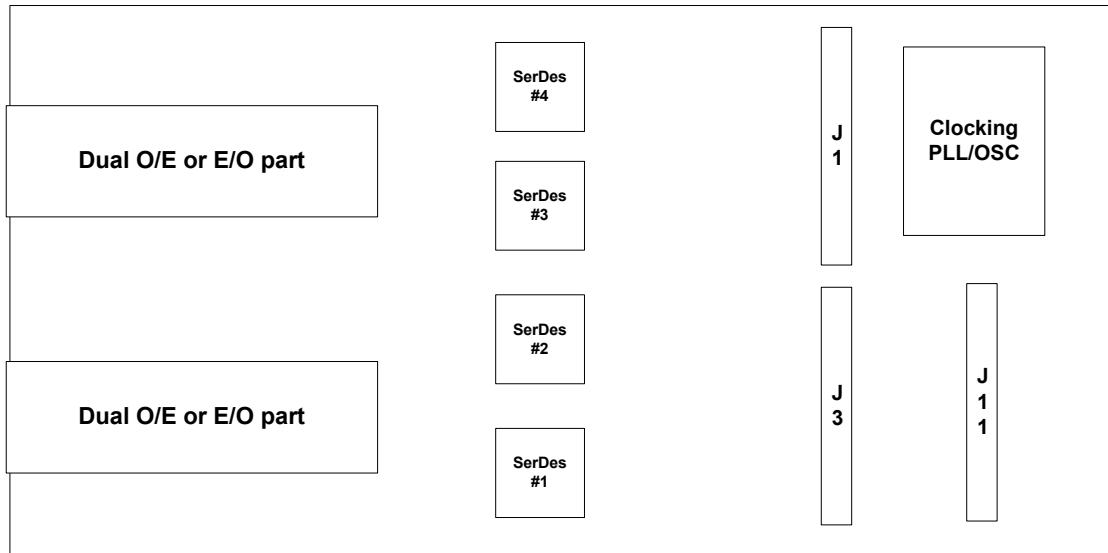
IMPLEMENTATION

The plan to instrument the optical links includes the production of two mezzanine cards which are based upon the Common Mezzanine Card (CMC) standard format. This card format was chosen not only for its convenience, but also its ability to be used with the CDF Pulsar module. The Pulsar module is used extensively in the CDF L2 system and provides a firmware programmable base upon which these mezzanine cards can be used and tested.

Due to the fact we want to plug into the Pulsar, we are already somewhat constrained in how we assign the pins on the mezzanine connectors. All of this is explored in the Appendices A, C and D. In addition, we found that some additional functionality is desired within the Stereo XFT system, and have added a third connector (J13) to the two connectors (J1 and J3) which are used on the Pulsar card. This third connector will carry signals which give us more control over the individual mezzanine modules, but is not necessary to its operation when plugged into the Pulsar.



Rough Drawing of the TX Mezzanine Card



Rough Drawing of the RX Mezzanine Card

The 4-Channel Transmitter Mezzanine Requirements

The 4-channel transmitter module must provide the following functionality:

- Provide a full 16 bit data path which operates up to 1.25Gbps
- Provide full function of transmitter control ability. (i.e. control of TX_ER, TX_EN bits of TLK1501)
- Provide individual channel control of reset function. (ENABLE)
- Provide a copy of the system clock chosen to the motherboard. (GTX_CLK)
- Selectable capability to run off a x8 CDF_Clock frequency or an oscillator.

The 4-Channel Receiver Mezzanine Requirements

The 4-channel receiver module must provide the following functionality:

- Provide a full 16 bit data path which operates up to 1.25Gbps
- Provide access to the individual status bits. (RX_ER, RX_DV)
- Provide access to individual receiver clocks. (RX_CLK)
- Provide a copy of the system clock chosen to the motherboard. (GTX_CLK)
- Selectable capability to run off a x8 CDF_Clock frequency or an oscillator.

Pulsar Card ID Assignments

CARD_ID bit 3:0:

1 1 1 1 SLINK card or nothing plugged in

0 0 1 0 Hotlink Tx card plugged in

0 0 1 1 Hotlink Rx card plugged in

0 0 0 0 Taxi Tx card plugged in

0 0 0 1 Taxi Rx card plugged in

0 1 0 0 XFT Optical Tx

0 1 0 1 XFT Optical Rx

Appendix A – The Pulsar Mezzanine Information on the Pinouts

Pulsar Mezzanine Connector J1 (as currently mapped according to schematic page)

Pin #	Signal	Signal	Pin#
1	URL3_sparein3	URL2_sparein2	2
3	+3.3V	URL2_sparein1	4
5	LDERR#_HSCD2	URL2_sparein0	6
7	LDOWN#_HSCD1	GND	8
9	GND	UXOFF#_sparein4	10
11	LCLK	GND	12
13	GND	LWEN#_HSCD0	14
15	URESET#_sparein7	GND	16
17	UDW1_sparein8	UTD0#_sparein5	18
19	LCTRL#_HSCD3	UDW0_sparein6	20
21	LD31_HQ37	+3.3V	22
23	GND	LD30_HQ36	24
25	LD29_HQ35	LD28_HQ34	26
27	LD27_HQ33	GND	28
29	LD26_HQ32	LD25_HQ31	30
31	GND	LD24_HQ30	32
33	LD23_HQ27	LD22_HQ26	34
35	LD21_HQ25	GND	36
37	LD20_HQ24	LD19_HQ23	38
39	+3.3V	LD18_HQ22	40
41	LD17_HQ21	LD16_HQ20	42
43	LD15_HQ17	GND	44
45	LD14_HQ16	LD13_HQ15	46
47	GND	LD12_HQ14	48
49	LD11_HQ13	LD10_HQ12	50
51	LD9_HQ11	+3.3V	52
53	LD8_HQ10	LD7_HQ07	54
55	GND	LD6_HQ06	56
57	LD5_HQ05	LD4_HQ04	58
59	LD3_HQ03	GND	60
61	LD2_HQ02	LD1_HQ01	62
63	+3.3V	LD0_HQ00	64

Pulsar Mezzanine Connector J3 (as currently mapped according to schematic page)

Pin #	Signal	Signal	Pin#
1	EINW0#	GND	2
3	GND	+2.5v	4
5	EINR0#	+2.5v	6
7	FIFO_empty0	+2.5v	8
9	VCC	BUSMODE0#	10
11	BUSMODE1#	BUSMODE2#	12
13	BUSMODE3#	GND	14
15	GND	+3.3V	16
17	FIFO_full0	+3.3V	18
19	Rp0#	+3.3V	20
21	VCC	ENW1#	22
23	EINW2#	EMR1#	24
25	EINR2#	GND	26
27	GND	FIFO_empty1	28
29	FIFO_empty2	FIFO_full1	30
31	FIFO_full2	GND	32
33	GND	Rp1#	34
35	Rp2#	ENW3#	36
37	ENA#0	GND	38
39	VCC	do_test	40
41	ENA#1	ENR3#	42
43	ENA#2	GND	44
45	GND	FIFO_empty3	46
47	ENA#3	FIFO_full3	48
49	SVS0	GND	50
51	GND	WriteCLK	52
53	Rp3#	GND	54
55	SVS1	GND	56
57	VCC	SVS2	58
59	CDF_clk	SVS3	60
61	BISTEN	GND	62
63	GND	MReset	64

Pulsar Mezzanine Connector J1 – Mappable I/O (empty spaces available)

Pin #	Signal	Signal	Pin#
1			2
3	+3.3V		4
5			6
7		GND	8
9	GND		10
11	*	GND	12
13	GND		14
15		GND	16
17			18
19			20
21		+3.3V	22
23	GND		24
25			26
27		GND	28
29			30
31	GND		32
33			34
35		GND	36
37			38
39	+3.3V		40
41			42
43		GND	44
45			46
47	GND		48
49			50
51		+3.3V	52
53			54
55	GND		56
57			58
59		GND	60
61			62
63	+3.3V		64

* parallel termination on Pulsar motherboard

Controlled impedance lines of Pulsar 58 +/-5 ohms

Parallel termination uses 180 ohms, 100 ohms pulled to +5V and GND

Pulsar Mezzanine Connector J3 - Mappable I/O (empty spaces available)

Pin #	Signal	Signal	Pin#
1		GND	2
3	GND	+2.5v	4
5		+2.5v	6
7	*	+2.5v	8
9	VCC	CARD_ID_0#	10
11	CARD_ID_1#	CARD_ID_2#	12
13	CARD_ID_3#	GND	14
15	GND	+3.3V	16
17		+3.3V	18
19		+3.3V	20
21	VCC		22
23			24
25		GND	26
27	GND	*	28
29	*		30
31		GND	32
33	GND		34
35			36
37		GND	38
39	VCC		40
41			42
43		GND	44
45	GND	*	46
47			48
49		GND	50
51	GND	**	52
53		GND	54
55		GND	56
57	VCC		58
59	CDF_Clock		60
61		GND	62
63	GND		64

* parallel termination on the motherboard

** serial termination on the motherboard

Appendix B – A look at the TLK1501 signal pins

TLK1501 – pin list

Signal Name	Type	Notes	Needed on RX Mezzanine	Needed on TX Mezzanine
DINRXN DINRXP	Input	O/E to RX pins	Internal use	
DOUTTXN DOUTTXP	Output	TX pins to E/O		Internal use
ENABLE	Input	used for reset	yes	yes
GTX_CLK	Input	input clock/output ref (driven by OSC onboard/offboard?)	yes	yes – output GTX_CLK back to control FPGA
LCKREFN	Input	set with jumper	no	no
LOOPEN	Input	set with jumper	no	no
PRBSEN	Input	set with jumper	no	no
RREF	Input	set with resistor	no	no
RXD(15:0)	Outputs		yes	no
RX_CLK	Output	output clock	yes	no
RX_ER/PRBS_PASS	Output	status bit	yes	no
RX_DV/LOS	Output	status bit	yes	no
TESTEN	Input	set with jumper	no	no
TXD(15:0)	Inputs		no	yes
TX_EN	Input	protocol bit	no	yes
TX_ER	Input	protocol bit	no	yes
VDD	pwr			
VDDA	pwr			
GND	gnd			
GNDA	gnd			

Appendix C – Mapping the 4 channel RX Pins

RX Mezzanine Connector J1 – Mapped for 4 channel RX

Pin #	Signal	Signal	Pin#
1	2_RXD(5)	2_RXD(4)	2
3	+3.3V	2_RXD(3)	4
5	2_RXD(2)	2_RXD(1)	6
7	2_RXD(0)	GND	8
9	GND	3_RX_CLK	10
11	GTX_CLOCK	GND	12
13	GND	3_RX_ER	14
15	3_RX_DV	GND	16
17	3_RXD(15)	3_RXD(14)	18
19	3_RXD(13)	3_RXD(12)	20
21	3_RXD(11)	+3.3V	22
23	GND	3_RXD(10)	24
25	3_RXD(9)	3_RXD(8)	26
27	3_RXD(7)	GND	28
29	3_RXD(6)	3_RXD(5)	30
31	GND	3_RXD(4)	32
33	3_RXD(3)	3_RXD(2)	34
35	3_RXD(1)	GND	36
37	3_RXD(0)	4_RX_ER	38
39	+3.3V	4_RX_DV	40
41	4_RXD(15)	4_RXD(14)	42
43	4_RXD(13)	GND	44
45	4_RXD(12)	4_RXD(11)	46
47	GND	4_RXD(10)	48
49	4_RXD(9)	4_RXD(8)	50
51	4_RXD(7)	+3.3V	52
53	4_RXD(6)	4_RXD(5)	54
55	GND	4_RXD(4)	56
57	4_RXD(3)	4_RXD(2)	58
59	4_RXD(1)	GND	60
61	4_RXD(0)	4_RX_CLK	62
63	+3.3V	1234_ENABLE	64

RX Mezzanine Connector J3 - Mapped for 4 channel RX

Pin #	Signal	Signal	Pin#
1	1_RX_CLK	GND	2
3	GND	+2.5v	4
5	1_RX_ER	+2.5v	6
7	1_RX_DV	+2.5v	8
9	VCC	CARD_ID_0#	10
11	CARD_ID_1#	CARD_ID_2#	12
13	CARD_ID_3#	GND	14
15	GND	+3.3V	16
17	1_RXD(15)	+3.3V	18
19	1_RXD(14)	+3.3V	20
21	VCC	1_RXD(13)	22
23	1_RXD(12)	1_RXD(11)	24
25	1_RXD(10)	GND	26
27	GND	1_RXD(9)	28
29	1_RXD(8)	1_RXD(7)	30
31	1_RXD(6)	GND	32
33	GND	1_RXD(5)	34
35	1_RXD(4)	1_RXD(3)	36
37	1_RXD(2)	GND	38
39	VCC	1_RXD(1)	40
41	1_RXD(0)	2_RX_ER	42
43	2_RX_DV	GND	44
45	GND	2_RXD(15)	46
47	2_RXD(14)	2_RXD(13)	48
49	2_RXD(12)	GND	50
51	GND	2_RXD(11)	52
53	2_RXD(10)	GND	54
55	2_RXD(9)	GND	56
57	VCC	2_RXD(8)	58
59	CDF_CLOCK	2_RXD(7)	60
61	2_RXD(6)	GND	62
63	GND	2_RX_CLK	64

RX Mezzanine Connector J13 - Mapped for 4 channel RX

Pin #	Signal	Signal	Pin#
1	ACTIVE ¹	OSC_ON	2
3	GND	GND	4
5	2_RX_Sig_Det	1_RX_Sig_Det	6
7	4_RX_Sig_Det	3_RX_Sig_Det	8
9	GND	GND	10
11	2_ENABLE	1_ENABLE	12
13	4_ENABLE	3_ENABLE	14
15	GND	GND	16
17	2_LOOPEN	1_LOOPEN	18
19	4_LOOPEN	3_LOOPEN	20
21	GND	GND	22
23	2_PRBSEN	1_PRBSEN	24
25	4_PRBSEN	3_PRBSEN	26
27	GND	GND	28
29	RESET		30
31			32
33			34
35			36
37			38
39			40
41			42
43			44
45			46
47			48
49			50
51			52
53			54
55			56
57			58
59			60
61			62
63			64

1 The signal ACTIVE will have a weak pulldown on the mezzanine module. The signal will be high asserted when it is plugged in a motherboard (XFT Stereo Finder or new TDC Optical Transition module). When the module is plugged into the Pulsar, the ACTIVE signal will remain low, indicating that the J13 connector is not in use.

Appendix D – Mapping the 4 channel TX Pins

TX Mezzanine Connector J1 – Mapped for 4 channel TX

Pin #	Signal	Signal	Pin#
1	2_TXD(5)	2_TXD(4)	2
3	+3.3V	2_TXD(3)	4
5	2_TXD(1)	2_TXD(2)	6
7	2_TXD(0)	GND	8
9	GND	3_ENABLE	10
11	GTX_CLOCK	GND	12
13	GND	3_TX_EN	14
15	3_TX_ER	GND	16
17	3_TXD(15)	3_TXD(14)	18
19	3_TXD(13)	3_TXD(12)	20
21	3_TXD(11)	+3.3V	22
23	GND	3_TXD(10)	24
25	3_TXD(9)	3_TXD(8)	26
27	3_TXD(7)	GND	28
29	3_TXD(6)	3_TXD(5)	30
31	GND	3_TXD(4)	32
33	3_TXD(3)	3_TXD(2)	34
35	3_TXD(1)	GND	36
37	3_TXD(0)	4_TX_EN	38
39	+3.3V	4_TX_ER	40
41	4_TXD(15)	4_TXD(14)	42
43	4_TXD(13)	GND	44
45	4_TXD(12)	4_TXD(11)	46
47	GND	4_TXD(10)	48
49	4_TXD(9)	4_TXD(8)	50
51	4_TXD(7)	+3.3V	52
53	4_TXD(6)	4_TXD(5)	54
55	GND	4_TXD(4)	56
57	4_TXD(3)	4_TXD(2)	58
59	4_TXD(1)	GND	60
61	4_TXD(0)	4_ENABLE	62
63	+3.3V	1234_PRBSEN	64

TX Mezzanine Connector J3 - Mapped for 4 channel TX

Pin #	Signal	Signal	Pin#
1	1_ENABLE	GND	2
3	GND	+2.5v	4
5	1_TX_EN	+2.5v	6
7	1_TX_ER	+2.5v	8
9	VCC	CARD_ID_0#	10
11	CARD_ID_1#	CARD_ID_2#	12
13	CARD_ID_3#	GND	14
15	GND	+3.3V	16
17	1_TXD(15)	+3.3V	18
19	1_TXD(14)	+3.3V	20
21	VCC	1_TXD(13)	22
23	1_TXD(12)	1_TXD(11)	24
25	1_TXD(10)	GND	26
27	GND	1_TXD(9)	28
29	1_TXD(8)	1_TXD(7)	30
31	1_TXD(6)	GND	32
33	GND	1_TXD(5)	34
35	1_TXD(4)	1_TXD(3)	36
37	1_TXD(2)	GND	38
39	VCC	1_TXD(1)	40
41	1_TXD(0)	2_TX_EN	42
43	2_TX_ER	GND	44
45	GND	2_TXD(15)	46
47	2_TXD(14)	2_TXD(13)	48
49	2_TXD(12)	GND	50
51	GND	2_TXD(11)	52
53	2_TXD(10)	GND	54
55	2_TXD(9)	GND	56
57	VCC	2_TXD(8)	58
59	CDF_CLOCK	2_TXD(7)	60
61	2_TXD(6)	GND	62
63	GND	2_ENABLE	64

TX Mezzanine Connector J13 - Mapped for 4 channel TX

Pin #	Signal	Signal	Pin#
1	ACTIVE ¹	OSC_ON	2
3	GND	GND	4
5	1_TX_DIS	1_PRBSEN	6
7	1_LOOPEN	1_RX_ER	8
9	GND	GND	10
11	2_TX_DIS	2_PRBSEN	12
13	2_LOOPEN	2_RX_ER	14
15	GND	GND	16
17	3_TX_DIS	3_PRBSEN	18
19	3_LOOPEN	3_RX_ER	20
21	GND	GND	22
23	4_TX_DIS	4_PRBSEN	24
25	4_LOOPEN	4_RX_ER	26
27	GND	GND	28
29	RESET		30
31			32
33			34
35			36
37			38
39			40
41			42
43			44
45			46
47			48
49			50
51			52
53			54
55			56
57			58
59			60
61			62
63			64

1 The signal ACTIVE will have a weak pulldown on the mezzanine module. The signal will be high asserted when it is plugged in a motherboard (XFT Stereo Finder or new TDC Optical Transition module). When the module is plugged into the Pulsar, the ACTIVE signal will remain low, indicating that the J13 connector is not in use.